

# EEPROM 128x8

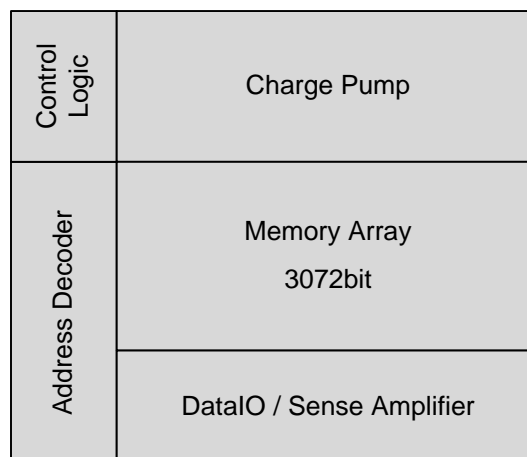
H35 – Memory IP – NVM



## Key Parameter

- Bits Organization 128x8 = 1024bit
- Number of Pages 32
- In/Out Bus Width 8bit
- Supply Voltage Write 2.3V to 5.5V
- Supply Voltage Read 2.3V to 5.5V
- Typ. Read Current 100µA @ 1MHz
- Typ. Write Current 85µA
- Write Time 6ms
- Read Access Time 100ns
- Block Area 0.54mm<sup>2</sup>

## Functional Block Diagram



## Process Characteristics

- Fabrication Process 0.35µm (H35EE)
- Process Option EEPROM midox
- Storage Element SimpleEE
- Temperature Range -40°C to 125°C
- Data Retention 20years at 125°C
- Write Cycles 100k cycles at 125°C

## Block Features

- Fixed memory building block
- Fully static RAM operation
- Fully differential sense amplifier
- Synchronous I/O interface

## General Description

The IP-block represents a non-volatile memory (NVM) device using a SimpleEE floating gate bit cell, intended for use in embedded micro controller systems. The movement of the charge in and out of the floating gate is done by the Fowler-Nordheim tunneling mechanism.

Access to the IP-block is similar to a static RAM, except the write access, which is more time consuming. To speed up write operations, the memory core is organized in 32 pages with 4 columns of 8bit each, where each write operation addresses one page.

The voltage required to program and to erase the memory cell is in the range of 14V, which is internally generated by an integrated Charge Pump.

A DataIO block with integrated Sense Amplifier together with the Address Decoder, Charge Pump and the Memory Array is managed by the Control Logic block. Special test modes for NVM bit cell screening are implemented and executed in the production test flow in order to ensure reliability of the NVM.

The device is optimized for low power operation by shutting down the sense amplifier after sensing the state of the bit cells.

For further information and requests, e-mail us at: [ip@ams.com](mailto:ip@ams.com)

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